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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,772	08/18/2003	Andre DeHon	B-5138NP 621046-7	3841

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EXAMINER	
GARBOWSKI, LEIGH M	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/643,772	DEHON ET AL.
	Examiner	Art Unit
	Leigh Marie Garbowski	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) *30-37 and 47-60* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,12-19,26,27,38,39 and 46* is/are rejected.

7)☒ Claim(s) *9-11,20-24,28,29 and 40-45* is/are objected to.

8)☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/22/4,4/11/5*. (6 sheets)
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Applicant's election with traverse of Group I Claims 1-29 and 38-46 in the reply filed on 12/12/2005 is acknowledged. The traversal is on the ground(s) that the restriction requirement is improper. This is not found persuasive because the inventions are patentably distinct as demonstrated by the reasoning given regarding subcombinations disclosed as usable together and process and apparatus for its practice. See also 37 CFR 1.141.

The requirement is still deemed proper and is therefore made FINAL.

Claim Objections

Claims 8 and 11 are objected to because of the following informalities: as per claim 8, there is no antecedent basis for "each repetition" [line 1]; as per claim 11, there is no antecedent basis for "the optimal element placement information" [line 1]. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7-8, 11-18, 25, 38-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Date et al. [U.S. Patent #5,144,563].

As per claim 1, a method of performing placement of a plurality of elements for electronic circuit design, comprising: a) providing a plurality of processing units, each processing unit of the plurality of processing units being able to communicate with one or more neighboring processing units of the plurality of processing units [column 5, lines 4-5]; b) establishing an initial placement for the elements by forming an initial association between each element and a processing unit [column 5, lines 15-16]; c) for each processing unit, in parallel, updating or not updating a list of processing units associated with the elements to be connected with the element associated with that processing unit [column 6, lines 23-36]; d) repeating step c) for a number of times [];

and e) for each processing unit, in parallel: e1) selecting a pairing processing unit to be paired with the processing unit [column 6, lines 3-12]; and e2) determining whether to exchange, between the processing unit and the pairing processing unit, the elements associated with the processing unit and the pairing processing unit [column 6, lines 3-22]. As per claim 2, wherein step e2) is a function of randomness and expected improvement of a cost function [column 6, lines 3-33; column 7, lines 38-43]. As per claim 3, wherein step e2) is a combination of a comparison between a randomly generated number and a parameter and a comparison of a value of a cost function after the exchange with a value of the cost function before the exchange [column 8, lines 27-29; column 6, lines 38-43]. As per claim 4, wherein step e2) is performed by means of a first comparing step wherein a randomly generated number is compared with a parameter and, in case the first comparing step is not satisfied, by means of a second comparing step where a value of a cost function after the exchange is compared with a value of the cost function before the exchange [column 8, lines 27-48; column 6, lines 38-43]. As per claim 7, wherein the processing units are disposed as a systolic array [column 5, lines 4-5, 44, 61; column 6, lines 3-7]. As per claim 8, wherein, for steps e1) and e2), a combination of steps e1) and e2) is performed up to four times, to pair each processing unit with all neighboring processing units able to communicate with that processing unit [column 6, lines 3-58]. As per claim 12, wherein the initial placement is established in a random manner [column 5, lines 15-17]. As per claim 13, wherein, in step e1), the pairing processing unit is selected among the one or more neighboring processing units [column 5, lines 4-5; column 6, lines 3-16]. As per claim 14, wherein step c) is repeated for a number of times equal to the number of processing units [column 9, lines 52-68]. As per claim 15, further comprising a step of outputting information indicating an optimal placement of said elements [column 8, lines 30-33, 62-66]. As per claim 16, wherein step c) further comprises: c1) communicating location information and identification information of an element to one of the one or more neighboring processing units [column 5, lines 35-45, 56-626; column 6, lines 3-60; column 7, lines 24-43]; and c2) receiving location information and identification information of an element from a different one of the one or more neighboring

processing units [column 6, lines 3-60; column 7, lines 24-43]. As per claim 17, further comprising a step of providing each processing unit with an initial list of elements to be connected with the element associated with that processing unit [column 6, line 64]. As per claim 18, further comprising: f) repeating steps e1) and e2) for a number of times; and g) repeating steps c through f) for a number of times [column 6, lines 45-58; column 7, lines 14-21]. As per claim 25, wherein step c) comprises providing timing information [column 1, lines 25-28].

As per claim 38, a method of performing placement of a plurality of elements for electronic circuit design, comprising: a) providing a plurality of processing units, each being able to be associated with one or more of the elements to be placed [column 5, lines 4-5]; b) for each processing unit: b1) selecting a pairing processing unit to be paired with the processing unit [column 6, lines 3-12]; and b2) determining whether to exchange, between the processing unit and the pairing processing unit, the elements associated with the processing unit and the pairing processing unit [column 6, lines 3-22]; c) for each processing unit, updating a list of processing units associated with the elements to be connected with the one or more elements associated with that processing unit [column 6, lines 23-36]. As per claim 39, wherein step b) is performed in parallel [column 5, lines 4-5].

Claims 1-8, 12-19, 25-27, 38-39, 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Scepanovic et al. [U.S. Patent #6,292,929 B2].

As per claim 1, a method of performing placement of a plurality of elements for electronic circuit design, comprising: a) providing a plurality of processing units, each processing unit of the plurality of processing units being able to communicate with one or more neighboring processing units of the plurality of processing units [column 15, lines 57-59; column 19, line 29]; b) establishing an initial placement for the elements by forming an initial association between each element and a processing unit [column 22, lines 59-65; column 23, lines 6-7]; c) for each processing unit, in parallel, updating or not updating a list of processing units associated with the elements to be connected with the element associated with that processing unit [column 21, line 65-column 22, line 59]; d) repeating step c) for a number of times [column 22, lines 55-59; column 23,

lines 36-40]; and e) for each processing unit, in parallel: e1) selecting a pairing processing unit to be paired with the processing unit [column 23, lines 23-27]; and e2) determining whether to exchange, between the processing unit and the pairing processing unit, the elements associated with the processing unit and the pairing processing unit [column 23, lines 27-35]. As per claim 2, wherein step e2) is a function of randomness and expected improvement of a cost function [column 17, lines 19-20]. As per claim 3, wherein step e2) is a combination of a comparison between a randomly generated number and a parameter and a comparison of a value of a cost function after the exchange with a value of the cost function before the exchange [column 16, lines 54-57; column 46, lines 51-52]. As per claim 4, wherein step e2) is performed by means of a first comparing step wherein a randomly generated number is compared with a parameter and, in case the first comparing step is not satisfied, by means of a second comparing step where a value of a cost function after the exchange is compared with a value of the cost function before the exchange [column 38, line 44-column column 40, line 14; column 46, line 50-column 47, line 54]. As per claim 5, wherein the parameter is a variable parameter that changes over time [column 23, lines 50-60]. As per claim 6, wherein the parameter decreases linearly over time [column 45, lines 34-36]. As per claim 7, wherein the processing units are disposed as a systolic array [column 15, lines 57-59]. As per claim 8, wherein, for steps e1) and e2), a combination of steps e1) and e2) is performed up to four times, to pair each processing unit with all neighboring processing units able to communicate with that processing unit [column 23, lines 37-39]. As per claim 12, wherein the initial placement is established in a random manner [column 3, lines 15-16, 39-40]. As per claim 13, wherein, in step e1), the pairing processing unit is selected among the one or more neighboring processing units [column 21, line 65; column 23, lines 23-27]. As per claim 14, wherein step c) is repeated for a number of times equal to the number of processing units [column 22, lines 55-59; column 23, lines 36-40]. As per claim 15, further comprising a step of outputting information indicating an optimal placement of said elements [column 26, lines 12-13]. As per claim 16, wherein step c) further comprises: c1) communicating location information and identification information of an element to one of the one or

more neighboring processing units [column 21, line 65-column 22, line 59]; and c2) receiving location information and identification information of an element from a different one of the one or more neighboring processing units [column 21, line 65-column 22, line 59]. As per claim 17, further comprising a step of providing each processing unit with an initial list of elements to be connected with the element associated with that processing unit [column 23, lines 6-8]. As per claim 18, further comprising: f) repeating steps e1) and e2) for a number of times; and g) repeating steps c through f) for a number of times [column 22, lines 55-59; column 23, lines 36-40]. As per claim 19, wherein step c) is performed by means of a position update chain [column 32, lines 16-17]. As per claim 25, wherein step c) comprises providing timing information [column 38, lines 46-51]. As per claim 26, wherein update information and timing information are simultaneously provided to the processing units [column 22, lines 55-59; column 23, lines 36-40; column 38, lines 44-51]. As per claim 27, wherein the cost function is a bounding box [Abstract].

As per claim 38, a method of performing placement of a plurality of elements for electronic circuit design, comprising: a) providing a plurality of processing units, each being able to be associated with one or more of the elements to be placed [column 15, lines 57-59; column 19, line 29]; b) for each processing unit: b1) selecting a pairing processing unit to be paired with the processing unit [column 23, lines 23-27]; and b2) determining whether to exchange, between the processing unit and the pairing processing unit, the elements associated with the processing unit and the pairing processing unit [column 23, lines 27-35]; c) for each processing unit, updating a list of processing units associated with the elements to be connected with the one or more elements associated with that processing unit [column 21, line 65-column 22, line 59]. As per claim 39, wherein step b) is performed in parallel [column 15, lines 57-59]. As per claim 46, wherein the number of processing units provided is inferior to the number of elements to be placed, and wherein placement is performed by means of a folding approach, wherein each processing unit is able to be associated with more than one element [column 46, line 50-column 47, line 54].

Allowable Subject Matter

Claims 9-11, 20-24, 28-29, 40-45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Date et al. [U.S. Patent #5,200,908] disclose placement optimizing [column 3, lines 63-67; column 4, lines 23-37; column 5, lines 9-15; column 8, lines 29-33, 50-54.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893 and e-mail is Leigh.Garbowski@uspto.gov. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LEIGH M. GARBOWSKI
PRIMARY EXAMINER